IN THE CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a low resistance embedded wiring layer formed on and extending over a semiconductor substrate; and

a plurality of element regions formed over the embedded wiring layer separated from one another and having at least one circuit element formed therein, each element region being in contact with the embedded wiring layer.

2. The semiconductor device of claim 1, wherein:

the plurality of element regions includes at least one supply element region in contact with the embedded wiring layer and receiving a predetermined power source potential.

3. The semiconductor device of claim 1, further including:

an insulating layer formed between the embedded wiring layer and the semiconductor substrate;

the embedded wiring layer is electrically connected to the semiconductor substrate through at least one opening in the insulating layer; and

the semiconductor substrate receives a predetermined power source potential.

4. The semiconductor device of claim 1, wherein:

the at least one circuit element includes a transistor having a source region, drain region, and channel region formed in the element region, the channel region being situated between each of the source and drain regions and the embedded wiring layer.

5. The semiconductor device of claim 1, wherein:

the least one circuit element includes a transistor having a source region, drain region, and channel region formed in the element region, the channel region being situated between one of the source and drain regions, and the other of the source and drain regions being electrically connected to the embedded wiring layer.

6. The semiconductor device of claim 1, wherein:

the least one circuit element includes a transistor having a source region, drain region, and channel region formed in the element region, the element region being surrounded by at least one insulating layer except for a bottom portion thereof, the source and drain regions being in contact with the at least one insulating layer and not in contact with the embedded wiring layer.

7. A semiconductor device, comprising:

a low resistance first embedded wiring layer and a low resistance second embedded wiring layer both formed on and extending over a semiconductor substrate, the first embedded wiring layer supplied with a first potential and the second embedded wiring layer supplied with a second potential different than the first potential;

a plurality of first element regions in contact with the first embedded wiring layer, each having at least one circuit element formed therein; and

a plurality of second element regions in contact with the second embedded wiring layer, each having at least one circuit element formed therein.

8. The semiconductor device of claim 7, wherein:

the plurality of first element regions includes at least one first supply element region in contact with the first embedded wiring layer and receiving the first potential; and

the plurality of second element regions includes at least one second supply element region in contact with the second embedded wiring layer and receiving the second potential.

9. The semiconductor device of claim 7, further including:

an insulating layer formed between the first and second embedded wiring layers and the semiconductor substrate;

the first potential is supplied to at least one first supply element region

in contact with the first embedded wiring; and

the second embedded wiring layer is electrically connected to the semiconductor substrate through at least one opening in the insulating layer, and the semiconductor substrate receives the second potential.

10. The semiconductor device of claim 7, wherein:

the at least one circuit element formed in the plurality of first element regions comprises a first conductivity type transistor; and

the at least one circuit element formed in the plurality of second element regions comprises a second conductivity type transistor.

11. The semiconductor device of claim 7, wherein:

the first embedded wiring layer is connected to a bottom surface of at least one first element region through bottom contact holes formed through a bottom insulating layer and a top wiring is connected to a top surface of the at least one first element region through top source/drain contact holes aligned over the bottom contact holes.

12. The semiconductor device of claim 7, wherein:

the at least one circuit element formed in the plurality of first element regions comprises a field effect transistor having a first source/drain region, a second source/drain region, and a channel region; and

the first embedded wiring layer contacts the first source/drain region

and the channel region, and does not contact the second source/drain region.

13. The semiconductor device of claim 7, wherein:

at least one circuit element formed in the plurality of first element regions comprises a field effect transistor having a first source/drain region, a second source/drain region, and a channel region, the first and second source/drain regions extending from a top surface of the first element region to a bottom surface of the first element region; and

the first embedded wiring layer contacts the channel region, and does not contact the first or second source/drain regions.

14. The semiconductor device of claim 7, wherein:

the low resistance first embedded wiring layer and the low resistance second embedded wiring layer comprise a metal.

15. A method of manufacturing a semiconductor device, comprising the steps of:

forming a silicon-on-insulator (SOI) type substrate that includes a first semiconductor substrate, a first insulating film formed over the semiconductor substrate, and a semiconductor layer formed over the first insulating film;

forming at least one insulated gate field effect transistor (IGFET) in a portion of the semiconductor layer separated from other portions of the semiconductor layer by isolation regions of the SOI type substrate;

planarizing the first semiconductor substrate to expose the first

insulating film;

removing at least a portion of the first insulating layer to expose the semiconductor layer;

forming a first conductive layer in contact with the first insulating film and the semiconductor layer;

forming a second conductive layer on a second semiconductor substrate;

bonding the SOI type substrate to the second semiconductor substrate with the first conductive layer in contact with the second conductive layer; and

heat treating the SOI type substrate and the second semiconductor substrate to fuse the first conductive layer to the second conductive layer.

16. The method of claim 15, further including:

patterning the first conductive layer to form a first wiring;

forming a second insulating film that covers the first insulating layer and the first wiring, and planarizing the resulting surface to expose the first wiring;

patterning the second conductive layer to form a second wiring;

forming a fourth insulating film that covers the second insulating layer and second wiring, planarizing a resulting surface to expose the second wiring;

bonding the SOI type substrate to the second semiconductor substrate

includes bonding the first wiring to the second wiring; and

heat treating the SOI type substrate and the second semiconductor substrate fuses the first wiring to the second wiring.

17. The method of claim 15, wherein:

forming the at least one IGFET includes etching holes through a top insulating films with a source/drain contact hole mask; and

removing at least a portion of the first insulating layer to expose the semiconductor layer includes etching through the first insulating layer with a mask developed from the source/drain contact hole mask.

18. The method of claim 15, wherein:

the other portions of the semiconductor layer include at least one supply portion coupled to a power source potential.

19. The method of claim 15, wherein:

forming the SOI type substrate includes

oxidizing a surface of the first semiconductor substrate,

oxidizing a surface of a third semiconductor substrate,

bonding the oxidized surface of the first semiconductor substrate to the oxidized surface of the third semiconductor substrate, and

planarizing the third semiconductor substrate to form the

semiconductor layer.

20. The method of claim 15, wherein:

forming the SOI type substrate includes implanting oxygen into a semiconductor substrate to form the first insulating film of silicon oxide, the portion of the semiconductor substrate below the first insulating film being the first semiconductor substrate, the portion of the semiconductor substrate above the first insulating film being the semiconductor layer.